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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/082,581	05/21/1998	KENJI NAGASE	980673	2888

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EXAMINER
WHIPKEY, JASON T

ART UNIT	PAPER NUMBER
2612	17

DATE MAILED: 07/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/082,581	NAGASE, KENJI	
	Examiner	Art Unit	
	Jason T. Whipkey	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 May 1998* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The proposed substitute sheets of drawings, filed on April 29, 2003, have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Response to Arguments

2. Applicant's arguments filed April 29, 2003, have been fully considered but they are not persuasive.

3. Regarding claims 5, 7, and 8, Applicant argues:

> In Preis, the voltage U2 output from the terminal b and the voltage U4 output from the terminal a are both produced from the output of the converter 2. In contrast, in the present invention of claim 5, the second voltage is generated by the fly-back circuit, but the first voltage in a voltage prior to being input to the fly-back circuit. That is, as different from Preis, the present invention has an advantage that the starting characteristic of the high-voltage circuit, i.e., fly-back circuit can be improved.

Page 7, lines 6-11. The examiner agrees with the first sentence, though he adds that the output from terminal "a" is first passed through the fly-back circuit consisting of diode 44 and capacitor 45 (Figure 1) prior to reaching terminal "a", as stated in item 13 of the Office action mailed January 29, 2003. Ergo, Preis anticipates Applicant's invention, as

recited in claim 5 and described in the second and third sentences quoted above. The presence of transformer 2 is irrelevant, since it alone does not form a fly-back circuit.

Applicant has amended claims 5 and 8 to include the limitation "as power outputs of the power supply circuit". The examiner notes that the addition of this limitation does not overcome the Preis reference, because, as Applicant argued in the above quotation, "the voltage U2 output from the terminal b and the voltage U4 output from the terminal a" are both produced as *outputs* of Preis's circuit.

4. Regarding claims 1 and 4, Applicant argues:

> Therefore, it is clear from the language of the claim that a short circuit for short-circuiting substantially between said positive polarity voltage outputting terminal and said negative polarity voltage outputting terminal only occurs in response to a power-off signal. In the outstanding Office Action, there if not mentioning of a power-off signal. Naturally, there is also no mentioning of short-circuiting in response to a power-off signal.

Page 8, lines 9-13. Though not explicitly stated in the Office action, it is clear that the only signal present after the power has been removed is produced "[w]hen the AC voltage is removed[,] capacitor 24 charges, which allows current to flow through the emitter-collector junction of PNP bipolar junction transistor 28 . . ." (page 10, lines 3-5). In other words, the loss of power results in a current flow, i.e., the power-off signal.

As a result, capacitors 14 and 16 are short-circuited by transistor 28.

5. Applicant's arguments with respect to claim 6 have been considered but are moot in view of the new ground of rejection.

Claim Rejections - 35 USC § 112

6. In response to the amendment filed April 29, 2003, the rejection of claims 1-4 and 7 under 35 U.S.C. § 112, second paragraph, is withdrawn.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claim 5 is rejected under 35 U.S.C. 102(e) as being anticipated by Preis.

Preis discloses a power supply that includes an electronic switch 22 (Figure 1), which acts as a chopper circuit. Switch 22 "chops" the voltage produced by DC voltage source 11 by repeatedly switching on and off based on pulses from clock controlled control device 5 (column 3, lines 30-34).

Diode 44 and capacitor 45 form a fly-back circuit for boosting the voltage produced by electronic switch 22 and transformer 2. The voltage created by the fly-back circuit at second terminal "a" with respect to ground is greater than the positive voltage on first terminal "b", which is connected to the output of transformer 2 via diode

31. Specifically, the voltage at terminal "a" with respect to ground is equal to U4, which is equal to the voltage at terminal "b" with respect to ground (U2) plus an additional voltage U3 (column 4, lines 1-37).

Terminals "a" and "b" are connected with zener diode 46 (column 5, lines 29-34).

Claim Rejections - 35 USC § 103

9. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

10. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Josephson in view of Deaver.

Regarding claim 1, Josephson discloses a power supply circuit, shown in Figure 1, with a first circuit for producing a positive polarity voltage at +12 V and +5 V output terminals, shown on the right side of the figure. This first circuit consists of rectifier 48, which includes capacitors 62 and 66 (column 4, lines 41-50), and a chopper circuit, which consists of electrical switch means 44 and transistor switch 24. Switch 24 turns on and off repeatedly to create a "chopped" output from transformer 22 (column 3, lines 44-52, and column 4, lines 13-27).

A second circuit, consisting of rectifier 16, diode 110, and capacitors 114 and 118, produce a negative polarity voltage of -12 V at an output terminal, shown on the

right side of Figure 1. Ground terminal GND, also shown on the right side of Figure 1, provides a reference for the positive and negative terminals.

Josephson is silent with regard to including means for short-circuiting the positive and negative terminals upon loss of source power.

Deaver discloses a discharge circuit for capacitors in a power supply. The power supply shown in the figure includes a first circuit that generates a positive polarity voltage, consisting of the two diodes shown on the right of full-wave rectifier 12 and connected to the positive node. This node is connected to a capacitor 14. The positive polarity voltage is output via terminal +VOUT.

The power supply also includes a second circuit that generates a negative polarity voltage, consisting of the two diodes shown on the left of full-wave rectifier 12 and connected to the negative node. This node is connected to a capacitor 16. The positive polarity voltage is output via terminal +VOUT. The transformer 10 is center-tapped to ground. When the AC voltage is removed capacitor 24 charges, which allows current to flow through the emitter-collector junction of PNP bipolar junction transistor 28 (column 3, lines 62-65). This discharges capacitors 14 and 16 (column 3, lines 66-67).

As stated in column 1, lines 61-66, this serves the purpose of preventing the discharge of hazardous amounts of charge stored in the capacitors, which makes the power supply safer. For this reason, it would have been obvious at the time of invention to have Josephson include a discharge means between the positive terminals and the negative terminals.

Regarding claims 2 and 3, transistor 28 in Deaver is a switching element, and resistor 30 is a current-limiting element. Both are located between the positive and negative terminals.

11. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Josephson in view of Deaver and further in view of Preis.

Claim 4 may be treated like claim 1. Additionally, Josephson includes a first positive polarity terminal for outputting a +5V voltage, which was produced by the first circuit described in the rejection of claim 1. Josephson also includes a fly-back circuit, consisting of secondary transistor winding 28 and rectifying circuit 48, to increase the voltage produced by the source side of transformer 22. The +12V voltage produced is placed on a second positive polarity terminal.

Josephson is silent with regard to including a diode between the first and second positive polarity output terminals.

Preis discloses a power supply that includes an electronic switch 22 (Figure 1), which acts as a chopper circuit. Diode 44 and capacitor 45 form a fly-back circuit for boosting the voltage produced by electronic switch 22 and transformer 2. The voltage created by the fly-back circuit at second terminal "a" with respect to ground is greater than the positive voltage on first terminal "b", which is connected to the output of transformer 2 via diode 31. Specifically, the voltage at terminal "a" with respect to ground is equal to U4, which is equal to the voltage at terminal "b" with respect to ground (U2) plus an additional voltage U3 (column 4, lines 1-37).

Terminals "a" and "b" are connected with zener diode 46 (column 5, lines 29-34).

As stated in column 5, lines 29-34, the advantage to including a zener diode between the two positive output terminals is that the voltage on the terminals is stabilized and the voltage U3 on capacitor 45 is held at a specific value. For this reason, it would have been obvious at the time of invention to have Josephson include a diode between the two positive polarity output terminals.

12. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwamoto in view of Sawanobori and further in view of Takeda (U.S. Patent No. 5,475,500).

Iwamoto discloses a power supply circuit with a circuit generating a positive polarity voltage (3 and the node connecting to terminal V_{DD}; see column 2, lines 58-64), a terminal for outputting the positive voltage (V_{DD}), a circuit generating a negative polarity voltage (3, the node connecting to terminal V_{SS1}; see column 2, lines 58-64), and a terminal for outputting the negative voltage (V_{SS2}, when SW3 and SW4 are closed).

Iwamoto shows that capacitor C_2 (and therefore terminals V_{DD} and V_{SS2}, with voltages of +5V and -5V, respectively), shown in Figure 1, may be short-circuited via switch SW_5 upon power off (column 5, lines 43-51). This eliminates a residual voltage between the terminals (column 5, lines 51-53). Consequently, the significant teaching provided by Iwamoto is that short-circuiting two output terminals of a power supply eliminates a residual voltage between the terminals.

Iwamoto is silent with regard to using the power supply circuit with a CCD imager.

Sawanobori shows that CCD 15 uses a power supply 15 consisting of a 15V line and a -9V line (Drawing 1). When power is lost on -9V line S3, discharge circuit 18 discharges the line to prevent "deterioration or destruction of the image pickup element due to application of a negative voltage" (constitution, lines 15-21). Therefore, the significant teachings provided by Sawanobori are: (a) that CCDs may require power supplies outputting separate positive and negative voltages, and (b) that a discharge circuit may prevent deterioration of or destruction to a CCD.

A power supply, such as the one described by Iwamoto, may operate irrespective of the device to which it is attached. Additionally, CCDs may operate irrespective of the structure of the power supply to which it is connected, assuming it receives the correct voltage or voltages. Since CCDs need a power supply in order to function, which was the conclusion reached by teaching (a) of Sawanobori, it would have been obvious to one of ordinary skill in the art at the time of invention to connect a CCD to a power supply. Acknowledging the teaching of Iwamoto and teaching (b) of Sawanobori as described above, it would have been obvious to one of ordinary skill in the art at the time of invention to discharge two terminals because the discharge eliminates a residual voltage between two terminals, and a discharge circuit may prevent deterioration of or destruction to a CCD.

Iwamoto is silent with regard to including a microcomputer and using it to produce the power-off signal.

Takeda discloses an imaging device controlled by microcomputer 16. As shown in the flowchart of Figure 7B, when microcomputer 16 detects a power off command (column 7, lines 58-65), it initiates a shutdown procedure for power supply parts 2a, 4, and 5 (column 8, lines 28-41). An advantage to using a microcomputer to produce a power-off signal is that the circuitry used to control the signal may be reused during other operations, thus simplifying the hardware design. For this reason, it would have been obvious at the time of invention to have Iwamoto perform shutdown control using a microcomputer.

13. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sawanobori in view of Josephson and further in view of Preis.

Sawanobori shows that CCD 15 uses a power supply 15 consisting of a 15V line and a -9V line (Drawing 1). However, Sawanobori is silent with regard to the specifics of the operation of power supply 15.

Josephson discloses a power supply circuit, shown in Figure 1, with a first circuit for producing a positive polarity voltage at +12 V and +5 V output terminals, shown on the right side of the figure. This first circuit consists of rectifier 48, which includes capacitors 62 and 66 (column 4, lines 41-50), and a chopper circuit, which consists of electrical switch means 44 and transistor switch 24. Switch 24 turns on and off repeatedly to create a "chopped" output from transformer 22 (column 3, lines 44-52, and column 4, lines 13-27).

A second circuit, consisting of rectifier 16, diode 110, and capacitors 114 and 118, produce a negative polarity voltage of -12 V at an output terminal, shown on the right side of Figure 1.

Josephson includes a first positive polarity terminal for outputting a +5V voltage. Josephson also includes a fly-back circuit, consisting of secondary transistor winding 28 and rectifying circuit 48, to increase the voltage produced by the source side of transformer 22. The +12V voltage produced is placed on a second positive polarity terminal.

Since Sawanobori is silent with regard to the specific circuitry used in power supply 15, one skilled in the art would recognize that any power supply producing positive and negative DC outputs could be used. For this reason, it would have been obvious at the time of invention to have Sawanobori's camera system include a power supply like the one described by Josephson.

Josephson is silent with regard to including a diode between the first and second positive polarity output terminals.

Preis discloses a power supply that includes an electronic switch 22 (Figure 1), which acts as a chopper circuit. Diode 44 and capacitor 45 form a fly-back circuit for boosting the voltage produced by electronic switch 22 and transformer 2. The voltage created by the fly-back circuit at second terminal "a" with respect to ground is greater than the positive voltage on first terminal "b", which is connected to the output of transformer 2 via diode 31. Specifically, the voltage at terminal "a" with respect to

ground is equal to U4, which is equal to the voltage at terminal "b" with respect to ground (U2) plus an additional voltage U3 (column 4, lines 1-37).

Terminals "a" and "b" are connected with zener diode 46 (column 5, lines 29-34).

As stated in column 5, lines 29-34, the advantage to including a zener diode between the two positive output terminals is that the voltage on the terminals is stabilized and the voltage U3 on capacitor 45 is held at a specific value. For this reason, it would have been obvious at the time of invention to have Josephson include a diode between the two positive polarity output terminals.

14. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Josephson in view of Deaver and further in view of Preis.

Josephson discloses a power supply circuit, shown in Figure 1, with a first circuit for producing a positive polarity voltage at +12 V and +5 V output terminals, shown on the right side of the figure. This first circuit consists of rectifier 48, which includes capacitors 62 and 66 (column 4, lines 41-50), and a chopper circuit, which consists of electrical switch means 44 and transistor switch 24. Switch 24 turns on and off repeatedly to create a "chopped" output from transformer 22 (column 3, lines 44-52, and column 4, lines 13-27).

A second circuit, consisting of rectifier 16, diode 110, and capacitors 114 and 118, produce a negative polarity voltage of -12 V at an output terminal, shown on the right side of Figure 1.

Josephson includes a first positive polarity terminal for outputting a +5V voltage. Josephson also includes a fly-back circuit, consisting of secondary transistor winding 28 and rectifying circuit 48, to increase the voltage produced by the source side of transformer 22. The +12V voltage produced is placed on a second positive polarity terminal.

Josephson is silent with regard to including means for short-circuiting the positive and negative terminals upon loss of source power.

Deaver discloses a discharge circuit for capacitors in a power supply. The power supply shown in the figure includes a first circuit that generates a positive polarity voltage, consisting of the two diodes shown on the right of full-wave rectifier 12 and connected to the positive node. This node is connected to a capacitor 14. The positive polarity voltage is output via terminal +VOUT.

The power supply also includes a second circuit that generates a negative polarity voltage, consisting of the two diodes shown on the left of full-wave rectifier 12 and connected to the negative node. This node is connected to a capacitor 16. The positive polarity voltage is output via terminal +VOUT. The transformer 10 is center-tapped to ground. When the AC voltage is removed capacitor 24 charges, which allows current to flow through the emitter-collector junction of PNP bipolar junction transistor 28 (column 3, lines 62-65). This discharges capacitors 14 and 16 (column 3, lines 66-67).

As stated in column 1, lines 61-66, this serves the purpose of preventing the discharge of hazardous amounts of charge stored in the capacitors, which makes the power supply safer. For this reason, it would have been obvious at the time of invention

to have Josephson include a discharge means between the positive terminals and the negative terminals.

Josephson is silent with regard to including a diode between the first and second positive polarity output terminals.

Preis discloses a power supply that includes an electronic switch 22 (Figure 1), which acts as a chopper circuit. Diode 44 and capacitor 45 form a fly-back circuit for boosting the voltage produced by electronic switch 22 and transformer 2. The voltage created by the fly-back circuit at second terminal "a" with respect to ground is greater than the positive voltage on first terminal "b", which is connected to the output of transformer 2 via diode 31. Specifically, the voltage at terminal "a" with respect to ground is equal to U4, which is equal to the voltage at terminal "b" with respect to ground (U2) plus an additional voltage U3 (column 4, lines 1-37).

Terminals "a" and "b" are connected with zener diode 46 (column 5, lines 29-34).

As stated in column 5, lines 29-34, the advantage to including a zener diode between the two positive output terminals is that the voltage on the terminals is stabilized and the voltage U3 on capacitor 45 is held at a specific value. For this reason, it would have been obvious at the time of invention to have Josephson include a diode between the two positive polarity output terminals.

Conclusion

15. Applicant's amendment necessitated the new ground of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason T. Whipkey, whose telephone number is (703) 305-1819. The examiner can normally be reached Monday through Friday from 9 A.M. to 6:30 P.M. eastern daylight time, alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber, can be reached on (703) 305-4929. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communication and (703) 872-9315 for After Final communication.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703) 306-0377.

Response to this action should be mailed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to the appropriate number above for communications intended for entry. (For informal or draft communications, please label **"PROPOSED"** or **"DRAFT"**.)
Hand-delivered responses should be brought to the sixth floor receptionist of Crystal Park II, 2121 Crystal Drive in Arlington, Virginia.

JTW
JTW
July 2, 2003

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